



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION WASHINGTON, D.C. 20546

MAR 1 4 1975

REPLY TO ATTN OF: GP

TO:

KSI/Scientific & Technical Information Division

Attn: Miss Winnie M. Morgan

FROM:

GP/Office of Assistant General

Counsel for Patent Matters

SUBJECT:

Announcement of NASA-Owned U.S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code KSI, the attached NASA-owned U.S. Patent is being forwarded for abstracting and announcement in NASA STAR.

The following information is provided:

U.S. Patent No.

: 3,869,659

Government or

Corporate Employee

U.S. Government

Supplementary Corporate

Source (if applicable)

: GSC-11,844-1

NASA Patent Case No.

NOTE - If this patent covers an invention made by a <u>corporate</u> employee of a NASA Contractor, the following is applicable:

YES / NO /X/

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of column No. 617101920 the Specification, following the words "...with respect to an invention of ..."

Bonne 3. Wooner

Bonnie L. Woerner Enclosure



[45] Mar. 4, 1975

[54] CONTROLLABLE HI	GH VOLTAGE
SOURCE HAVING FA	ST SETTLING TIME

[75] Inventors: Henry Doong, Beltsville; Mario H. Acuna, Bowie, both of Md.

Acuna, Bowle, both of Md.

73] Assignee: The United States of America as represented by the Administration of

the National Aeronautics and Space Administration, Washington, D.C.

[22] Filed: Mar. 19, 1974

[21] Appl. No.: 452,761

[56]

[52] U.S. Cl...... 321/15, 307/227, 324/32

[58] Field of Search 321/15, 2; 324/32; 307/227

References Cited

30772

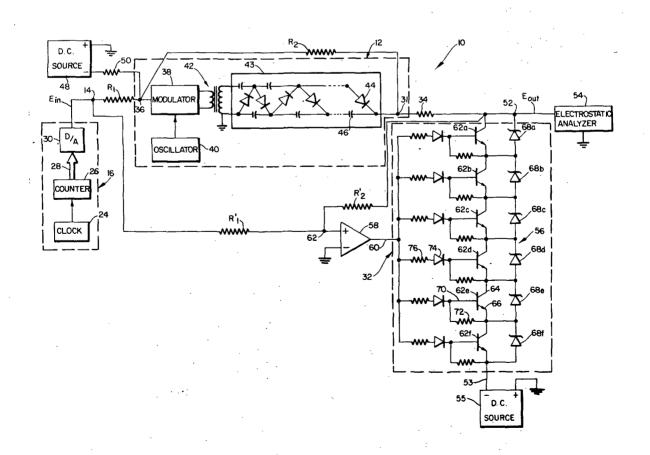
[50]	ije.	ici ciices Ciieu		
UNITED STATES PATENTS				
3,458,721	7/1969	Maynard	307/227	X
3,628,061	12/1971	Jackman	307/227	X
3,775,664	11/1973	Forstmeyer	321/	15

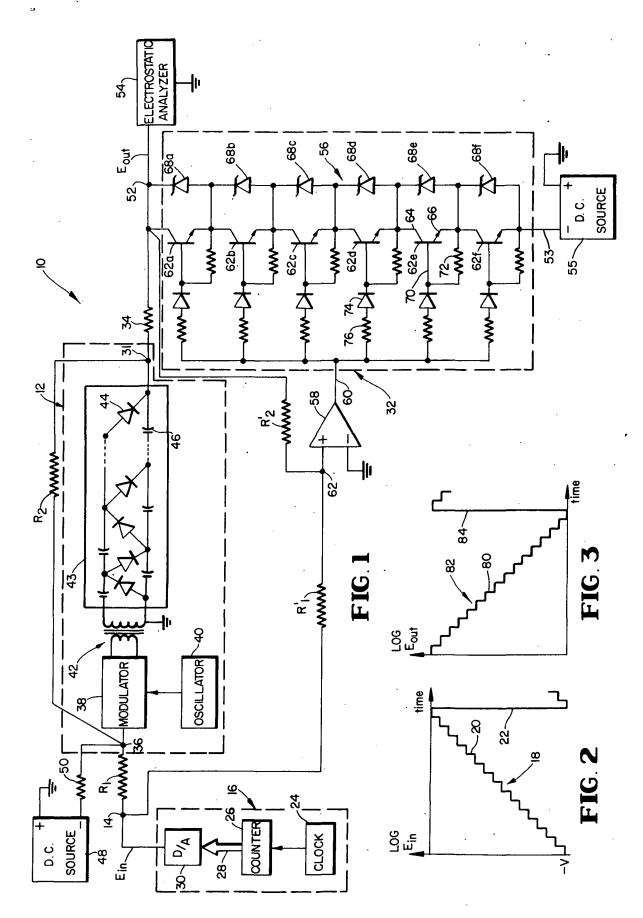
Primary Examiner—R. N. Envall, Jr. Attorney, Agent, or Firm—Robert F. Kempf; Ronald F. Sandler; John R. Manning

[57] ABSTRACT

A high voltage d.c. stepping power supply for sampling a utilization device such as an electrostatic analyzer has a relatively fast settling time for voltage steps. The supply includes a waveform generator for deriving a low voltage staircase waveform that feeds a relatively long response time power supply deriving a high output voltage generally equal to a predetermined multiple of the input voltage. In the power supply, an a.c. voltage modulated by the staircase waveform is applied to a step-up transformer and thence to a voltage multiplier stack to form a high voltage, relatively poor replica of the input waveform at an intermediate output terminal. A constant d.c. source, applied to the input of the power supply, biases the voltage at the intermediate output terminal to be in excess of the predetermined multiple of the input voltage. A fast shunt regulator responsive to the input signal provides an output which is a faithful high voltage reproduction of the staircase waveform. The shunt regulator includes a solid state shunt device connected to the intermediate output terminal via a dropping resistor. The supply output is taken from the junction of the resistor and the shunt device.

16 Claims, 3 Drawing Figures





1

CONTROLLABLE HIGH VOLTAGE SOURCE HAVING FAST SETTLING TIME

ORIGIN OF THE INVENTION

The invention described herein was made by employees of the United States Government and may be manufactured and used by or for the Government for governmental purposes without the payment of royalties thereon or therefor.

FIELD OF THE INVENTION

The present invention relates generally to high voltage controllable power supplies and to amplifiers for deriving a high voltage replica of an input signal. The present invention relates particularly to a fast response 15 time controllable power supply which is formed as the combination of a slow responding power supply and a fast responding shunt regulator.

BACKGROUND OF THE INVENTION

High voltage power supplies having a staircase output voltage waveform are used on board spacecraft as a deflection voltage source for electrostatic analyzers to sample the charged particle velocity distribution functions of a hot plasma viewed from the spacecraft. In 25 such an application, particularly in conjunction with a fast spinning spacecraft, it is highly desirable that the supply have both low power dissipation and a short settling time, on the order of 200 microseconds, for producing the staircase steps sufficiently fast to maximize spatial resolution and permit rapid precise measurement.

Prior art stepping power supplies with low power dissipation have generally been mechanized by modulating an a.c. source with an input staircase low voltage 35 waveform and applying the modulated a.c. to a step-up transformer followed by a voltage multiplier stack. These supplies, principally due to the characteristics of the voltage multiplier, have been unable to satisfy the aforementioned requirements for sampling a spacecraft 40 born electrostatic analyzer. Prior art supplies of this type with low power dissipation consistent with a spacecraft environment have generally had settling times between voltage steps on the order of 20 milliseconds. For the case of fast spinning spacecraft, this settling time can be as much as 100 times too slow. It is estimated that if the voltage multiplier of such a supply were designed to meet the settling time requirement, the resultant power supply would have a power dissipation of about 50 times that desired.

OBJECTS OF THE INVENTION

It is an object of the present invention to provide a controllable high voltage power supply having a fast response to an input signal.

It is another object of the present invention to provide a high voltage stepping power supply having both rapid settling time between steps and low power dissipation.

It is a further object of the present invention to provide a stepping power supply which is a reliable all solid state design.

SUMMARY OF THE INVENTION

The stepping high voltage power supply of the present invention, as in the prior art, comprises a waveform generator deriving a low voltage staircase waveform

2

which modulates an a.c. signal. The modulated a.c. signal is applied to a step-up transformer and voltage multiplier stack to form a high voltage unidirectional signal which is a predetermined multiple of said low voltage waveform.

In the present invention, in contradistinction to the prior art, the staircase waveform is biased with a d.c. source so that the output high voltage of the multiplier is in excess of the predetermined multiple of said input 10 signal. A shunt regulator rapidly responsive to said low voltage waveform includes shunt devices coupled to the voltage multiplier output via a dropping resistor across which is developed an output voltage equal to the predetermined multiple of the input waveform. For reliability, the shunt devices are solid state, comprising a plurality of transistors having emitter and collector electrodes connected in series to achieve the required voltage breakdown rating.

Because the capacitors of a voltage multiplier charge through forward biased diodes and discharge through back biased diodes, the output voltage of the multiplier can increase rather rapidly but can only decrease relatively slowly. Since the shunt regulator rapidly decreases the voltage of the multiplier, the result is a controllable power supply having rapid response for either increasing or decreasing the output voltage.

Other objects and features of the present invention will become apparent upon perusal of the following detailed description of one embodiment of the present invention taken in conjunction with the appended drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is an electrical schematic of the stepping power supply of the present invention.

FIG. 2 is a logarithmic versus linear plot of input voltage to the FIG. 1 supply, as a function of time.

FIG. 3 is a logarithmic versus linear plot of output voltage of the FIG. 1 supply, as a function of time.

DETAILED DESCRIPTION OF THE DRAWING

Referring to FIG. 1, the high voltage stepping power supply of the present invention includes a slow or long response time controllable power supply 12 having an input terminal 14 for receiving an input signal E_{IN} (FIG. 2) derived by a staircase waveform generator 16. The output of generator 16 is a positive going, staircase waveform including a portion 18, which generally rises from a maximum negative voltage -V (on the order of -5 volts) to zero volts in preferably 16 staircase steps 20 at varying amplitude, and a fly back portion 22 from zero volts to -V.

Waveform generator 16 comprises a clock source 24 which feeds a four stage binary counter 26 having a four bit parallel output 28 that is coupled to a four bit digital to analog converter 30 for deriving the voltage E_{IN} coupled to terminal 14. Clock source 24 preferably has a frequency on the order of 50 Hertz to provide 20 millisecond spaced voltage steps 20 that occur synchronously with pulses from the clock.

As will become apparent, long response time power supply 12 derives a positive output voltage at its output terminal 31; the output voltage has only one polarity and ranges from 100 volts to 1,600 volts, whereby a step is produced in response to each of the steps 20 of E_{IN} with a predetermined negative multiplication factor (gain) on the order of 300. As with prior art supplies

}

the power supply 12 has a settling time on the order of 20 milliseconds and has a tendency to follow, but does not faithfully reproduce, the waveform of E_{IN} at its output terminal 31. As will be better understood as the description proceeds, the present invention provides a 5 faithful reproduction of the E_{IN} waveform at terminal 52 by connecting dropping resistor 34 between terminals 31 and 52, across which is connected shunt regulator 32 that is driven by the output voltage of noninverting, d.c. feedback amplifier 58 responsive to the 10 voltage E_{IN} at terminal 14. The shunt regulator 32 has substantially only resistive components, i.e., no lumped inductances or capacitances, and thereby has a relatively fast response time.

 E_{IN} is coupled to a virtual ground input terminal 36 15 of power supply 12 via an input resistor R₁ connected between terminals 14 and 36. A feedback resistor R₂ is connected between virtual ground input terminal 36 and output terminal 31 providing power supply 12, a negative voltage gain given by the ratio of R₂ to R₁. Supply 12 is actually a d.c. to a.c. to d.c. converter and includes a modulator 38 that is fed by the signal on input terminal 36 and by the output of a high frequency sinusoidal oscillator 40, having a frequency typically on the order of 50 kilohertz. The output of modulator 38, a variable amplitude sinusoidal signal having an amplitude proportional to the d.c. signal on input terminal 36, is applied to a step-up transformer 42 to provide additional voltage gain. The a.c. output of step-up transformer 42 is applied to a conventional rectifying, voltage multiplier stack 43 comprising diodes 44 and capacitors 46. Voltage multiplier 43 derives a relatively high level, positive d.c. voltage that is supplied to output terminal 31.

To provide freedom for shunt regulator 32 to operate for positive and negative d.c. voltage variations, a negative d.c. source 48 is coupled to input terminal 36 via an input resistor 50 to bias the output voltage on terminal 31 to a voltage in excess of the voltage E_{IN} times the gain of supply 12. Preferably, d.c. source 48 and resistor 50 are chosen to bias the voltage on terminal 31 about 100 volts in excess of that given by the gain of supply 12 times E_{IN} . Thus, in the absence of d.c. source 48, the output voltage on terminal 31 would range from 45 0 to 1,500 volts; with d.c. source 48 chosen as indicated, the voltage on terminal 31 ranges from 100 to 1,600 volts.

The output voltage, Eour, derived between terminal 52 and ground, is applied to a utilization device such as 50 an electrostatic analyzer 54 of either the cylindrical or spherical type for sampling charged particle velocities of a hot plasma. While the output voltage of power supply 12 appearing at terminal 31 has poor settling time in response to the steps 20 of E_{IN} and has a positive d.c. bias due to source 48, E_{out} is a faithful reproduction of E_{IN} times a gain on the order of 300, i.e., E_{OUT} ranges from 0 to 1,500 volts in 16 proportional staircase steps. This faithful reproduction at terminal 52 is achieved by pulling the voltage at terminal 31 down in response to E_{IN} via dropping resistor 34 with the controllable shunt regulator 32 connected between terminal 51 and the negative terminal 53 of a positively grounded, low d.c. voltage source 55, typically having a voltage of 5 volts.

Shunt regulator 32 is controlled by high gain, noninverting amplifier 58 via amplifier output line 60. Amplifier 58 is in a path external to the series path of supply 12 (between terminal 14 and 52) and receives the

staircase waveform E_{IN} via an input resistor $R_{1'}$ connected between terminal 14 and a virtual ground input terminal 62 of the amplifier. Amplifier 58 also receives the stepping supply output voltage E_{OUT} as a feedback signal via resistor $R_{2'}$ connected between virtual ground input terminal 62 and output terminal 52. Shunt regulator 32 and amplifier 58 have a negative overall gain given by the ratio of $R_{2'}$ to $R_{1'}$, which is chosen to be the same as the ratio of R_{2} to R_{1} .

For high reliability purposes, shunt regulator 32 comprises all solid state elements. Because of the relatively high maximum voltage appearing at terminal 52, i.e., about 1,500 volts, and because of the limited breakdown voltage of available solid state devices, shunt regulator 32 comprises a plurality of NPN transistors 62 ("a" through "f") shunted by zener diodes 68 ("a" through "f"). Preferably there are six transistors 62, each having collector and emitter electrodes 64 and 66 connected in a series or totem pole arrangement between terminal 52 and the negative terminal 53 of d.c. source 55. The six transistors 62 are progressively labeled 62a to 62f from terminal 52 to source 55. Each transistor 62 has a breakdown voltage on the order of 400 volts. This arrangement permits the voltage E_{OUT} to be generally divided across the transistors 62 so that each transistor is not stressed above the breakdown voltage.

The collector and emitter electrodes 64 and 66 of each transistor are shunted by a separate zener diode, 68a to 68f, having a zener voltage selected in the range of about 250 to 300 volts to fix the maximum voltage across each transistor. The emitter electrode 66 and base electrode 70 of each transistor 62 are connected by a separate stabilizing resistor 72 for shunting transistor leakage current in a manner well known in the art. Each transistor base electrode 70 is coupled to amplifier output line 60 via a separate diode 74 in series with a current limiting resistor 76. Diodes 74 are poled to conduct current from line 60 into the base electrodes 70, thereby isolating the base voltages of the various transistors 62.

Shunt regulator 32 is variably driven into conduction by the output of amplifier 58 to reduce the voltage at terminal 52 below that of terminal 31 in response to E_{IN} . To this end, current is conducted out of supply 12 through dropping resistor 34 into shunt regulator 32 and passes serially from terminal 52 through a group of the zener diodes 68 and thence through a group of transistors 62 to the -5 volt return terminal of source 55. For the purpose of discussion it is assumed that zener diodes 68 have a zener voltage of 250 volts and that the instantaneous voltage of E_{OUT} is 1,200 volts. Starting from terminal 52, the first four zener diodes 68a to 68d are in conduction providing a voltage across diodes 68a to 68d of 1,000 volts, the remaining diodes (68e and 68f) and the first four transistors (62a to 62d) being cut off. The conduction path passes through the fifth and sixth transistors 62e and 62f, the former being dynamically controlled by the output of amplifier 58 so it has a collector-emitter voltage drop of approximately 200 volts and the latter being saturated and having a voltage drop approaching zero volts to produce the 1,200 volts from terminal 52 to ground. The first four transistors 68a to 68d are maintained cut off because the emitter voltages established by the first four zener diodes are higher than the small base voltage established by amplifier 58.

Thus, for any instantaneous voltage E_{OUT} , not more than one of transistors 62 is dynamically controlled by amplifier 58 while the transistors above the controlled transistor are cut off and the transistors below the controlled transistor are saturated. Each of the transistors 62 assumes control in different adjoining 250 volt ranges, whereby transistor 62f dynamically controls E_{OUT} between 0 and 250 volts, transistor 62e dynamically controls E_{OUT} between 250 volts and 500 volts, etc. The shunt regulator 32 is returned to the small negative voltage of source 55, rather than to ground, to enable a small saturation voltage of transistors 62 to be overcome so that E_{OUT} can be controlled in the neighborhood of zero volts.

What has been described is a completely solid state stepping power supply in which E_{OUT} , a high voltage replica of E_{IN} as shown in FIG. 3, has been obtained with a staircase portion 82 having settling times of 200 microseconds between steps 80, enabling rapid, precise sampling of electrostatic analyzer 54. Furthermore, the power supply 12, while capable of only slow discharge through back biased diodes 44, has the capability of a rapid charging because in that situation the diodes 44 are forward biased. This rapid charging ability provides a rising flyback portion 84 of E_{OUT} from 0 to 1,500 volts in about 2 milliseconds.

The invention has provided the combination of a controllable power supply having a relatively fast response only for increasing voltage and a shunt regulator 32 having a fast response for decreasing voltage. The provision of control to both power supply 12 and shunt regulator 32 allows the maximum voltage across the dropping resistor 34 to be kept rather small, about 100 volts, resulting in low power dissipation. Since the electrostatic analyzer 54 represents substantially an open circuit enabling resistor 34 to be several megohms, the power dissipation in resistor 34 is less than about 10 millimatts

Having described in detail a preferred embodiment 40 of the invention, it should be apparent that numerous modifications may be made to the embodiment within the spirit and scope of the invention. Hence, it is intended that the detailed description be considered as illustrative of the concept of the invention and not in 45 a limiting sense.

What is claimed is:

1. A controllable high voltage source having a relatively fast response to a low voltage input signal source with a predetermined gain comprising:

a pair of input terminals for said input signal source; a pair of output terminals for high voltage output;

- a relatively long response time controllable high voltage source coupled between said input and output terminals, said long response time source having said predetermined gain;
- means for d.c. biasing said long response time controllable voltage source to have an output voltage in excess of the input signal times said gain; and
- fast response time shunt regulator means coupled across said output terminals responsive to said input signal at said input terminals for reducing the output voltage across said output terminals to said gain times said input signal.
- 2. The apparatus of claim 1 wherein said long response time source includes a rectifying voltage multiplier responsive to an a.c. source and means for con-

trolling the amplitude of said a.c. source in response to said input signal.

- 3. The apparatus of claim 1 wherein said relatively long response time source has a relatively fast response for increasing said output voltage and a relatively slow response for decreasing said output voltage.
- 4. The apparatus of claim 2 wherein said output voltage has only one polarity and further including a source of relatively low d.c. voltage opposite in polarity to said output voltage, said shunt regulator means including a plurality of transistors having emitter and collector electrodes connected in series between one of said output terminals and said low voltage source.
- 5. The apparatus of claim 3 wherein said output voltage has only one polarity and further including a source of relatively low d.c. voltage opposite in polarity to said output voltage, said shunt regulator means including a plurality of transistors having emitter and collector electrodes connected in series between one of said output terminals and said low voltage source.
- 6. A high voltage stepping power supply having relatively fast settling time for voltage steps comprising:

a digital clock source;

means for deriving a low voltage staircase analog input voltage signal having steps synchronous with said clock source;

a pair of output terminals;

a relatively long response time controllable high voltage source responsive to said input voltage signal, said high voltage source having a predetermined gain, said high voltage source being coupled to said output terminals, means for d.c. biasing said high voltage source to have an output voltage in excess of said analog voltage times said gain; and

fast response time shunt regulator means responsive to said input signal coupled across said output terminals for reducing the output voltage at said output terminals to said gain times said input signal.

- 7. The apparatus of claim 6 wherein said high voltage source includes a rectifying voltage multiplier responsive to an a.c. source and means for controlling the amplitude of said a.c. source in response to said input signal
- 8. The apparatus of claim 6 wherein said high voltage source has a relatively fast response for increasing said output voltage and a relatively slow response for decreasing said output voltage.
- 9. The apparatus of claim 7 wherein said output voltage has only one polarity and further including a source of relatively low d.c. voltage opposite in polarity to said output voltage, said shunt regulator means including a plurality of transistors having emitter and collector electrodes connected in series between one of said output terminals and said low voltage source.
- 10. The apparatus of claim 8 wherein said output voltage has only one polarity and further including a source of relatively low d.c. voltage opposite in polarity to said output voltage, said shunt regulator means including a plurality of transistors having emitter and collector electrodes connected in series between one of said output terminals and said low voltage source.
- 11. A high voltage source having an output terminal for developing a high voltage capable of following relatively rapid variations of a relatively low voltage input source comprising an input terminal responsive to the input source, a series path between the input and output terminals said path including a d.c. to a.c. to d.c.

converter connected to be responsive to the voltage at the input terminal for deriving a high voltage output having a tendency to follow the variations, a variable impedance shunt path having substantially only resistive components connected across the output terminal, and means external to the first path responsive to the voltage at the input terminal for controlling the impedance of the shunt path.

12. The source of claim 11 wherein the converter includes a voltage multiplier having diodes and capaci- 10

13. The source of claim 12 further including a resistor series connected between the output of the converter and the output terminal, said means for controlling the impedance of the shunt path including a non- 15 inverting d.c. amplifier, said amplifier having an input terminal connected to be responsive to the input source and a feedback resistor connected between the output terminal and the amplifier input terminal.

14. The source of claim 13 wherein the shunt imped- 20 ance includes plural series connected variable impedance elements, each of said elements including means for enabling a (a) predetermined, finite voltage, (b) a substantially zero voltage and (c) dynamic voltage to be developed across them in response to the voltage at 25 the amplifier means for controlling the shunt path imthe output terminal, and means for dynamically controlling the voltage developed across only one of the

elements at a time in response to an output voltage of

15. The source of claim 14 further including a first input resistor between the relatively low voltage input terminal and the amplifier input terminal, a second input resistor between the relatively low voltage input terminal and an input terminal of the converter, and another feedback resistor between the converter output and the converter input terminals, the ratio of the input resistor to the feedback resistor for the amplifier being substantially equal to that for the converter so that the gain of the series path including the converter and the path including the amplifier are substantially the same.

16. The source of claim 12 wherein the shunt impedance includes plural series connected variable impedance elements, each of said elements including means for enabling a (a) predetermined, finite voltage, (b) a substantially zero voltage and (c) dynamic voltage to be developed across them in response to the voltage at the output terminal, and means for dynamically controlling the voltage developed across only one of the elements at a time in response to an output voltage of pedance.

30

35

40

45

50

55

60